Achieving the Ideal Testing on HDL Programs

[1]Onur Kılınççeker, [2]Ercüment Türk, [3]Moharram Challenger, [4]Fevzi Belli

Address:

[1,4]University of Paderborn,
Paderborn, Germany

[1]Muğla Sıtkı Koçman University,
Muğla, Turkey

[4]Izmir Institute of Technology,
Izmir, Turkey

[2,3]International Computer Institute,
Ege University, Izmir, Turkey

E-Mail: [1]okilinc@mail.upb.de
[4]belli@upb.de

Abstract

This paper proposes an adaptation of the Ideal Testing methodology for testing behavioral model of sequential circuits implemented in Hardware Description Language (HDL). The concept of Ideal Testing is adapted to achieve reliability and validity of by combining the holistic and mutation testing. The holistic testing requires a positive and a negative testing. The first step, test preparation, of the approach leads to a model of the given HDL represented by a Finite State Machine (FSM) that is then converted to a Regular Expression (RE). The second step, test generation and execution, the REs are used to construct test sequences for a positive and a negative testing. For a positive testing, the original (fault-free) FSM model is used, while for negative testing its mutant model(s) are used to define requirements of the Ideal Testing in conjunction with model based and code based mutation testing. A demonstrating example based on a Traffic Light Controller (TLC) confirms the proposed approach and analyzes its characteristic features.